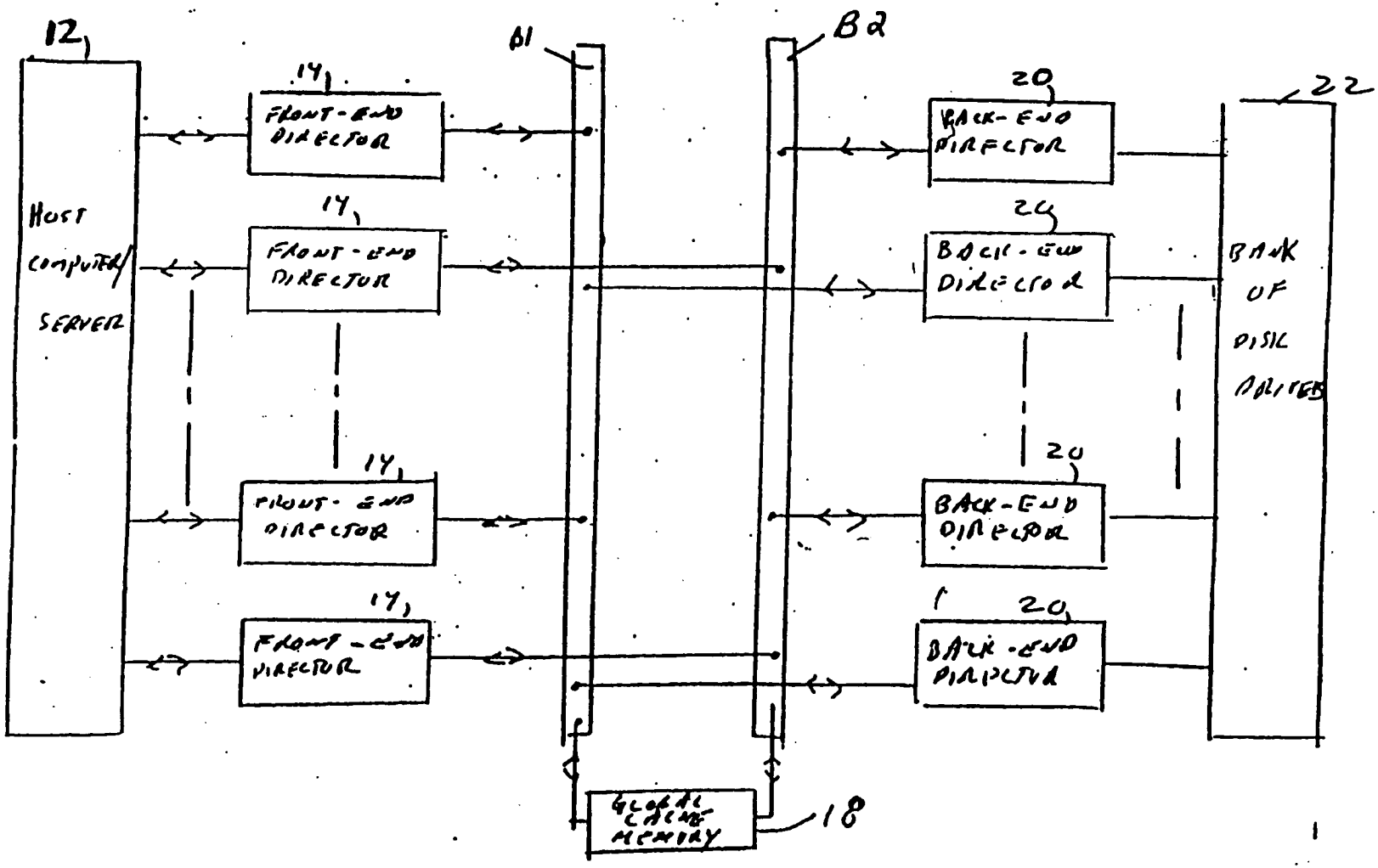
SCANNED, # 12

FIG. 1
PRIOR ART



SCANNED, # 12

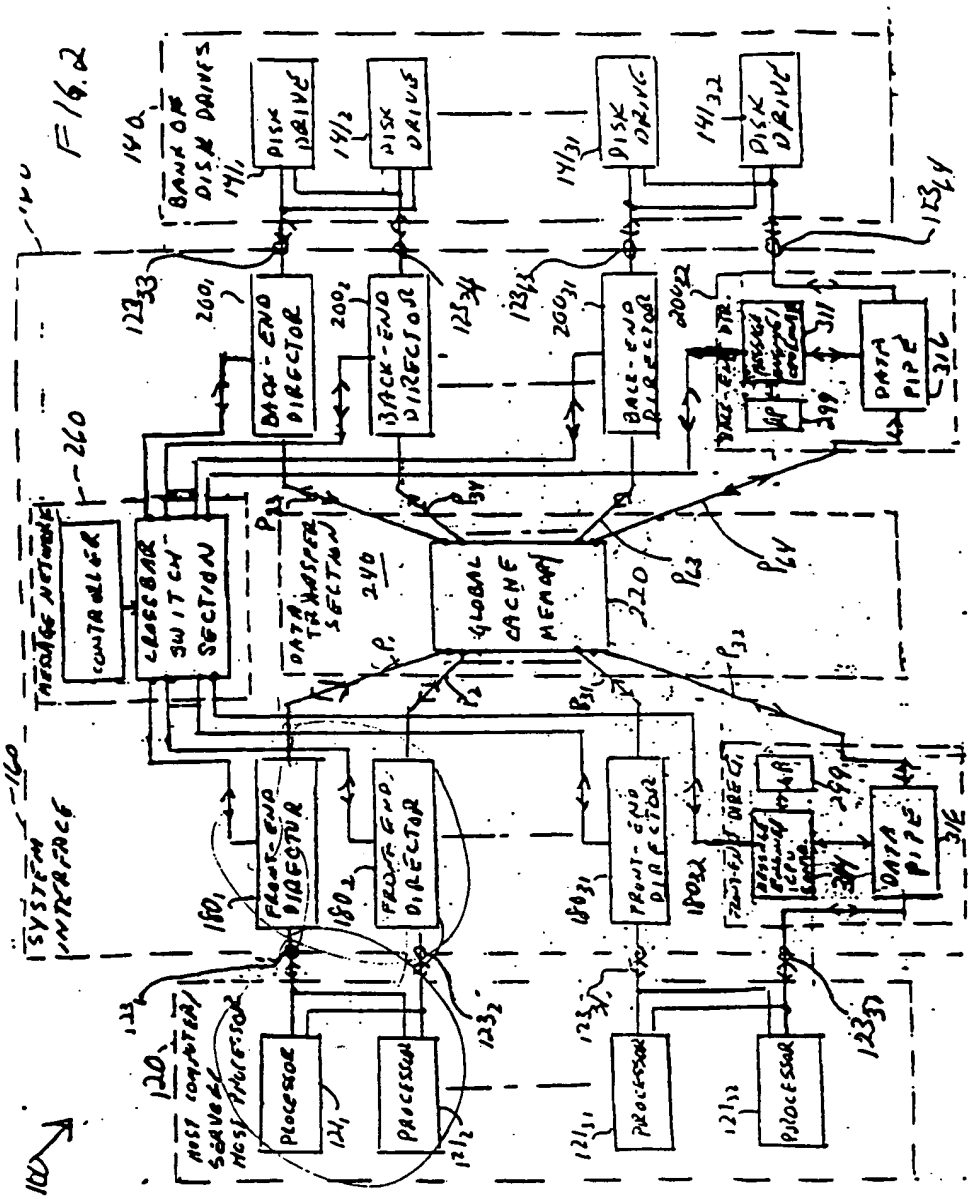


FIG. 2
DISK DRIVES
DISK DRIVE
BACK-END DIRECTOR
CROSSBAR SWITCH SECTION
CONTROLLER
DATA MOVER SECTION
GLOBAL CACHE MEMORY
FRONT-END DIRECTOR
DATA PIPE
PROCESSOR
HOST COMPUTER/ SERVER/ HOST PROCESSOR
SYSTEM INTERFACE
INTERCONNECT NETWORK

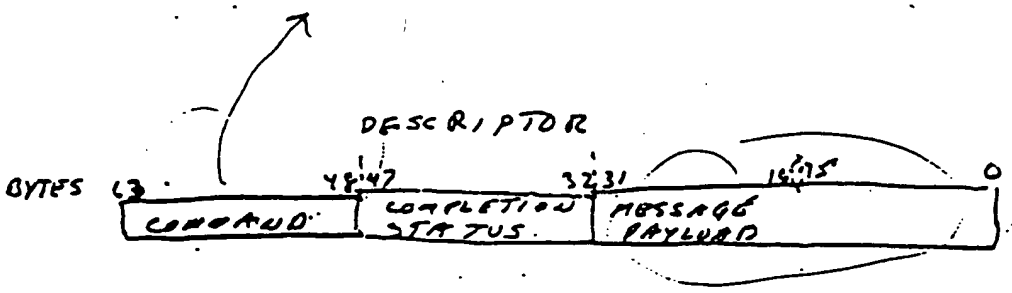

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

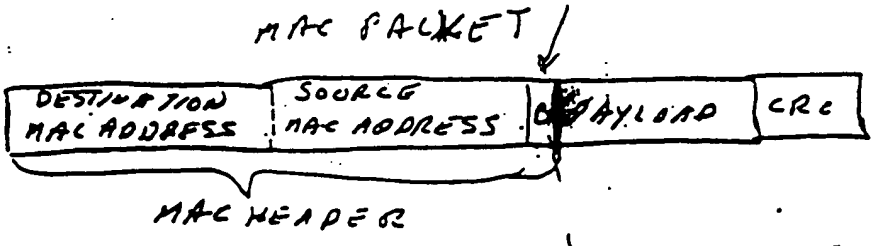

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

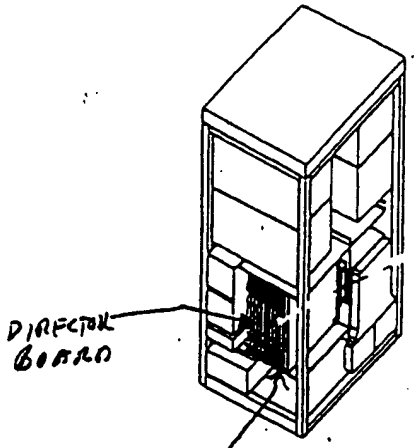
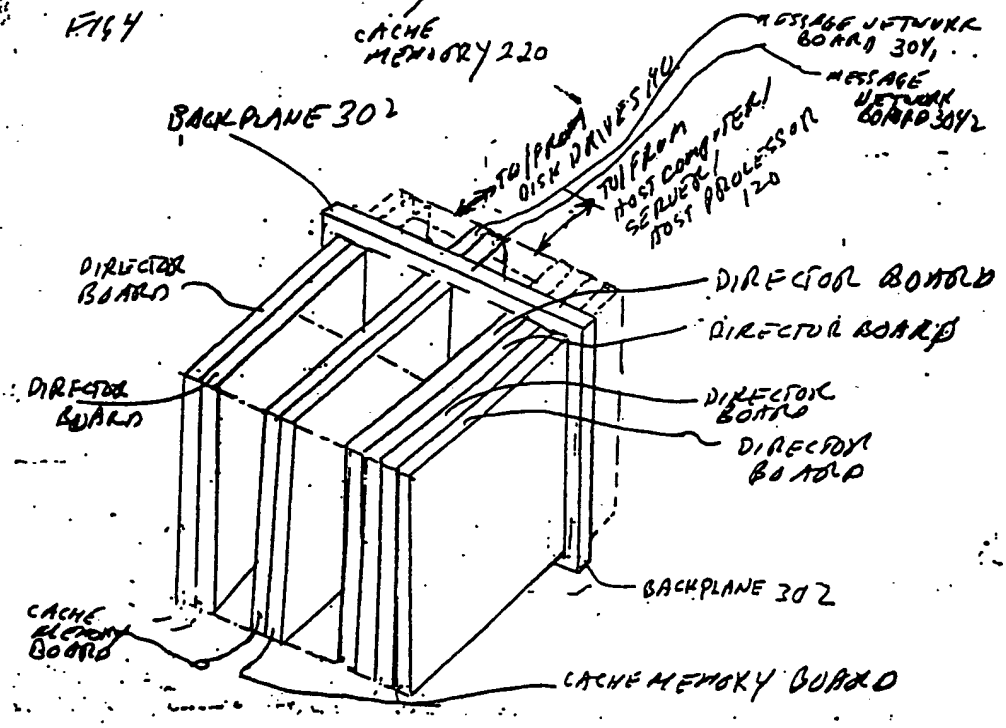
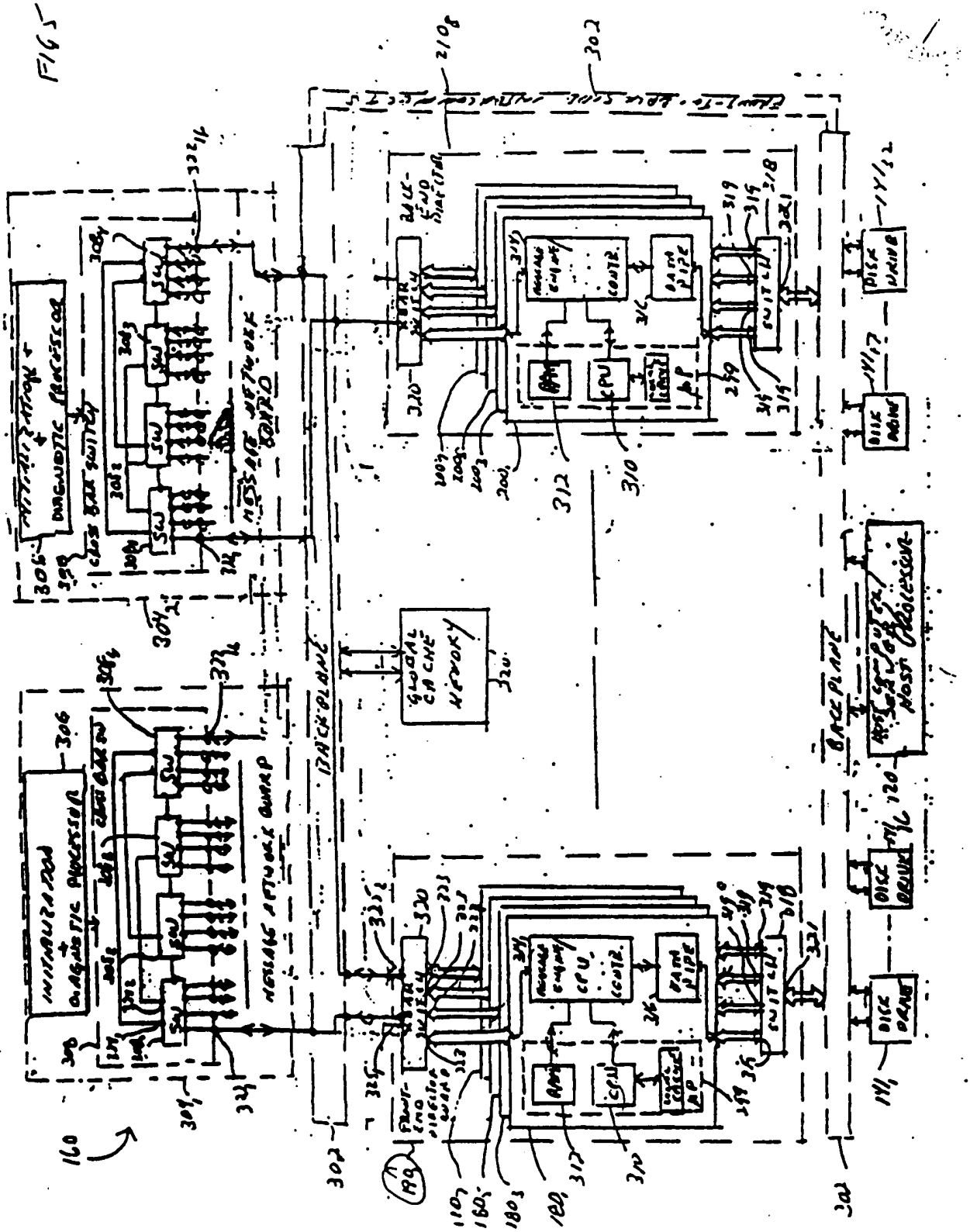
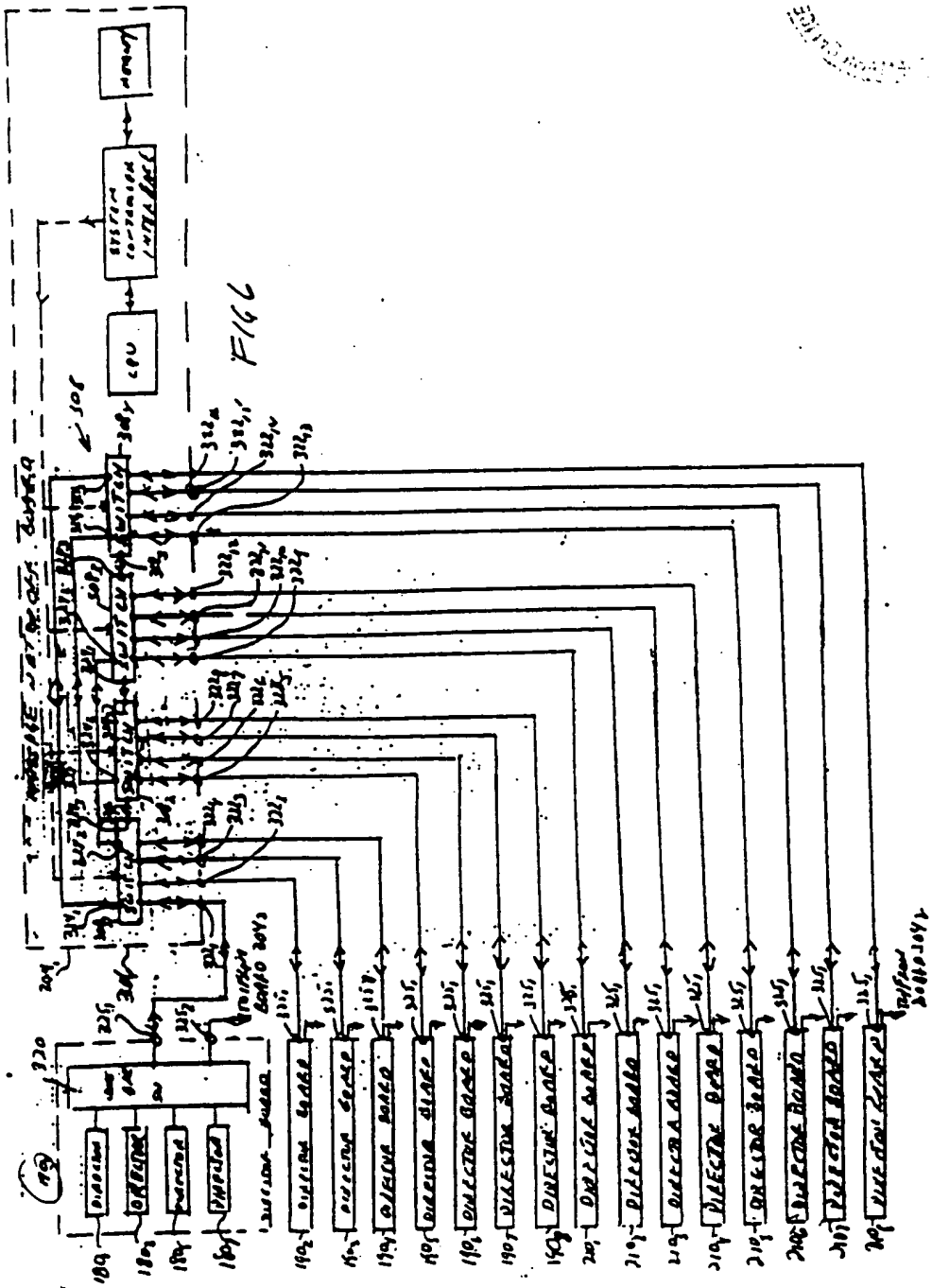

DIRECTOR
BOARD

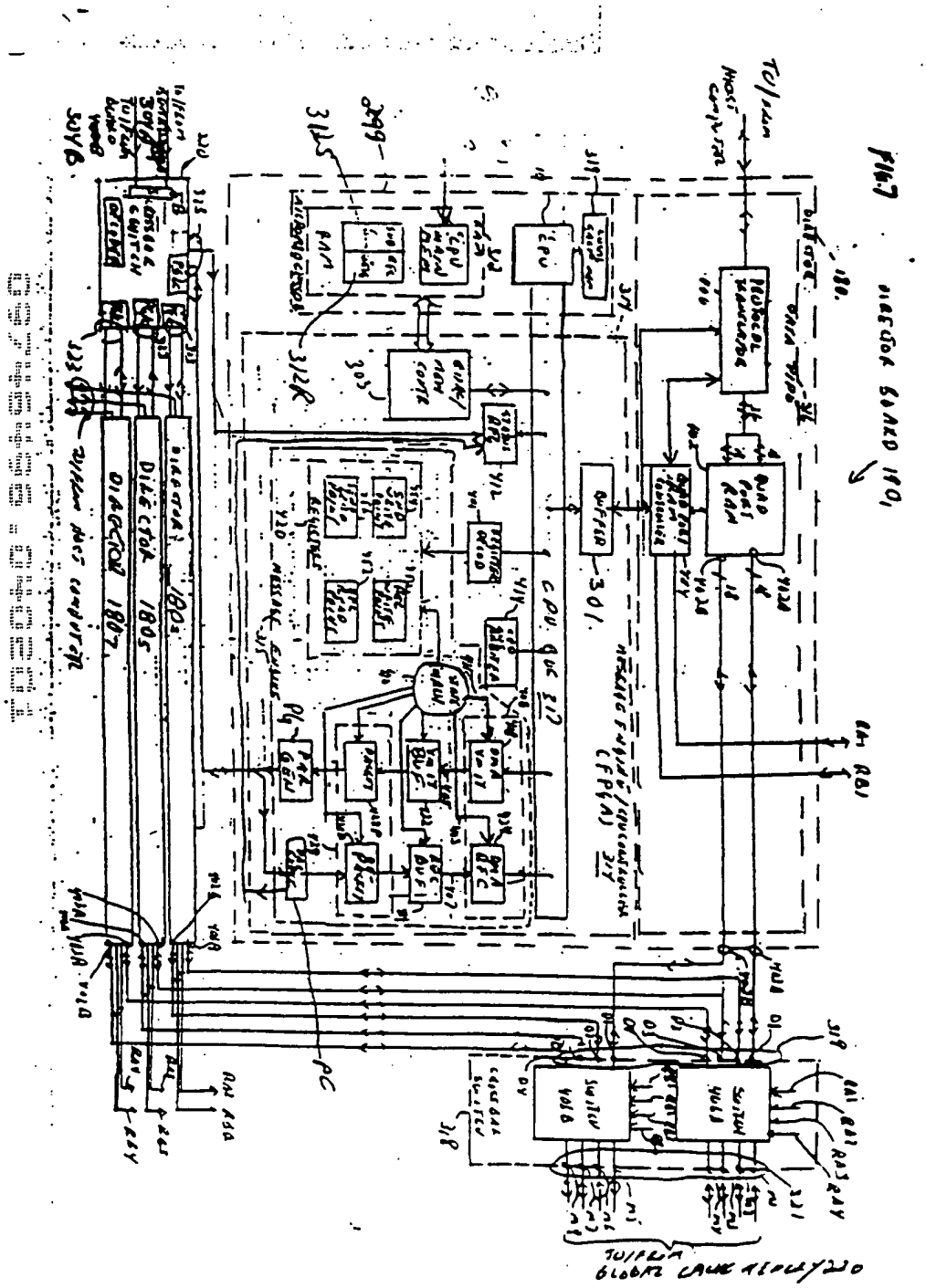
FIG. 3

FIG 4


CACHE MEMORY 220
MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD







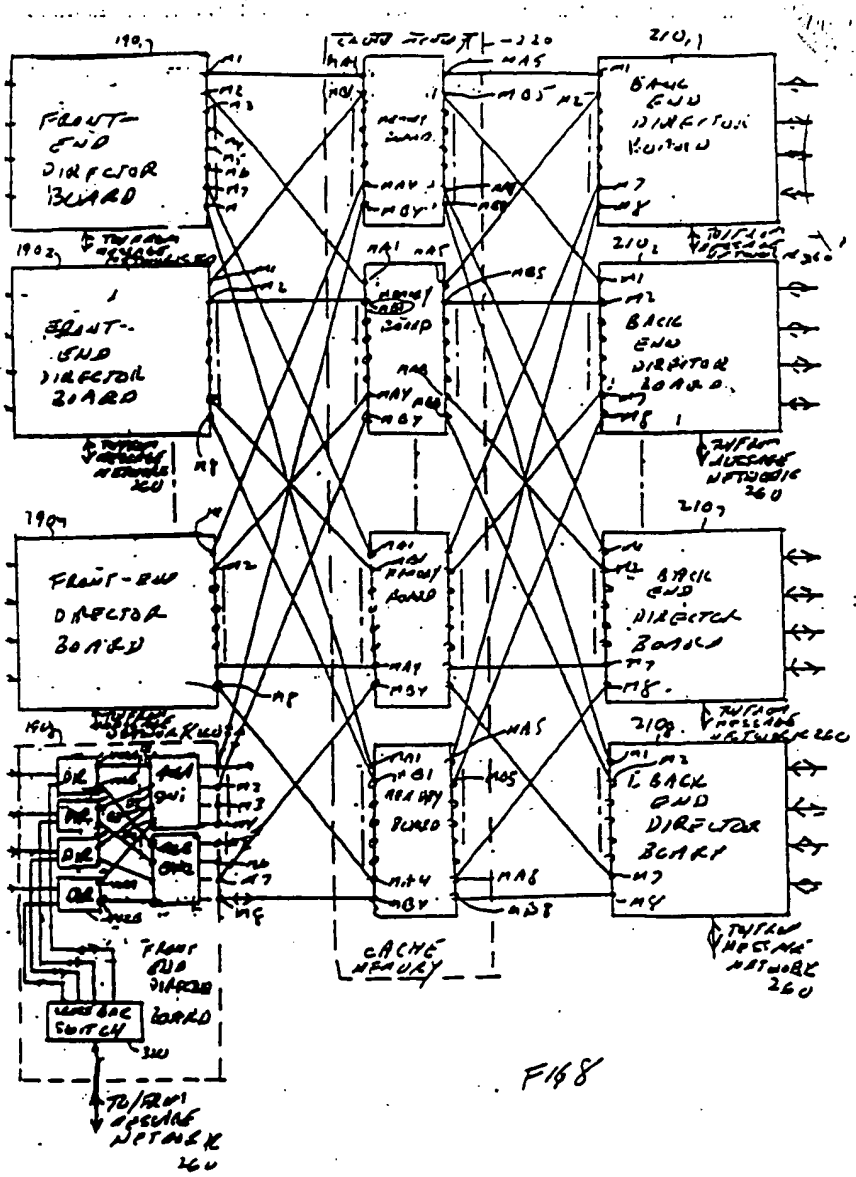

FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
SWITCH
FRONT END DIRECTOR BOARD
BACK END DIRECTOR BOARD

Fig 8

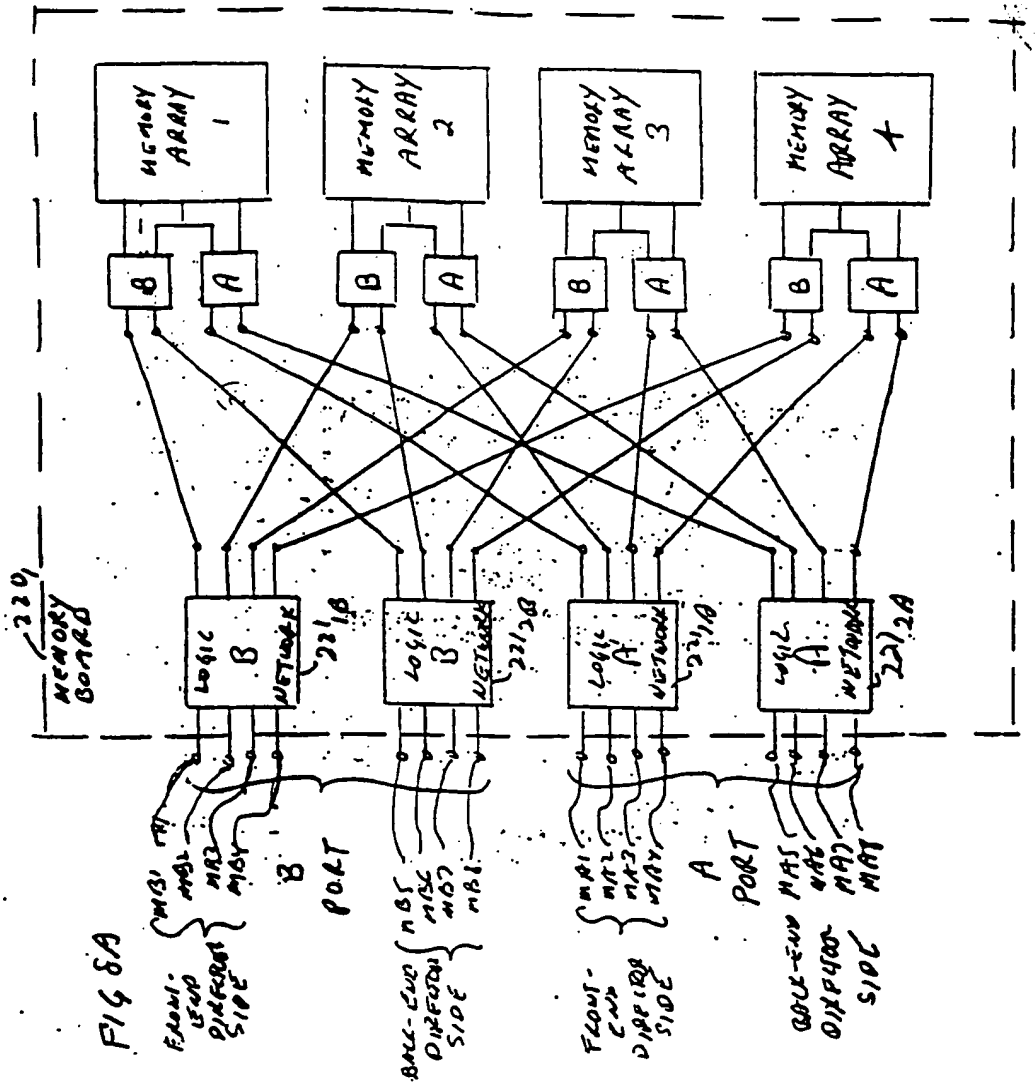

MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
220
MEMORY BOARD
LOGIC
NETWORK
221/1B
221/2B
221/3B
221/4A
B PORT
A PORT

FIG 6A

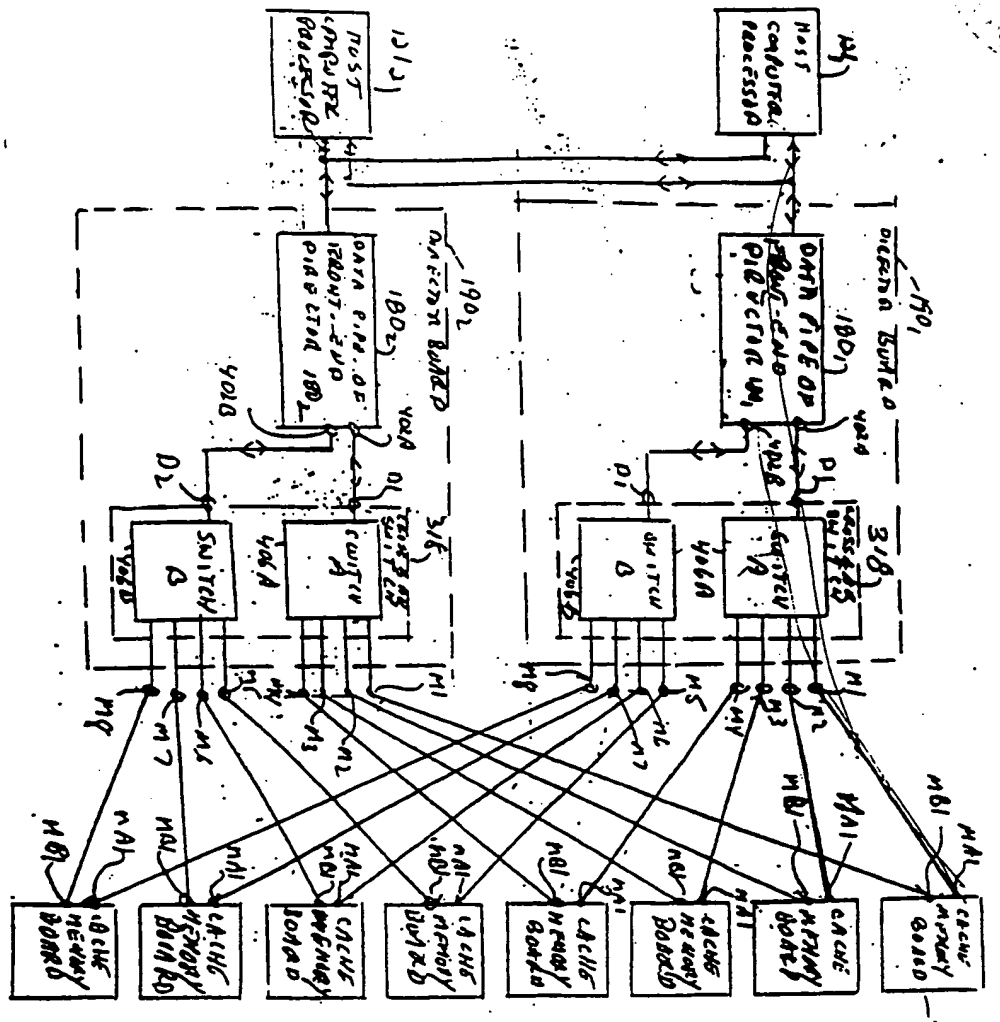


FIG 8B

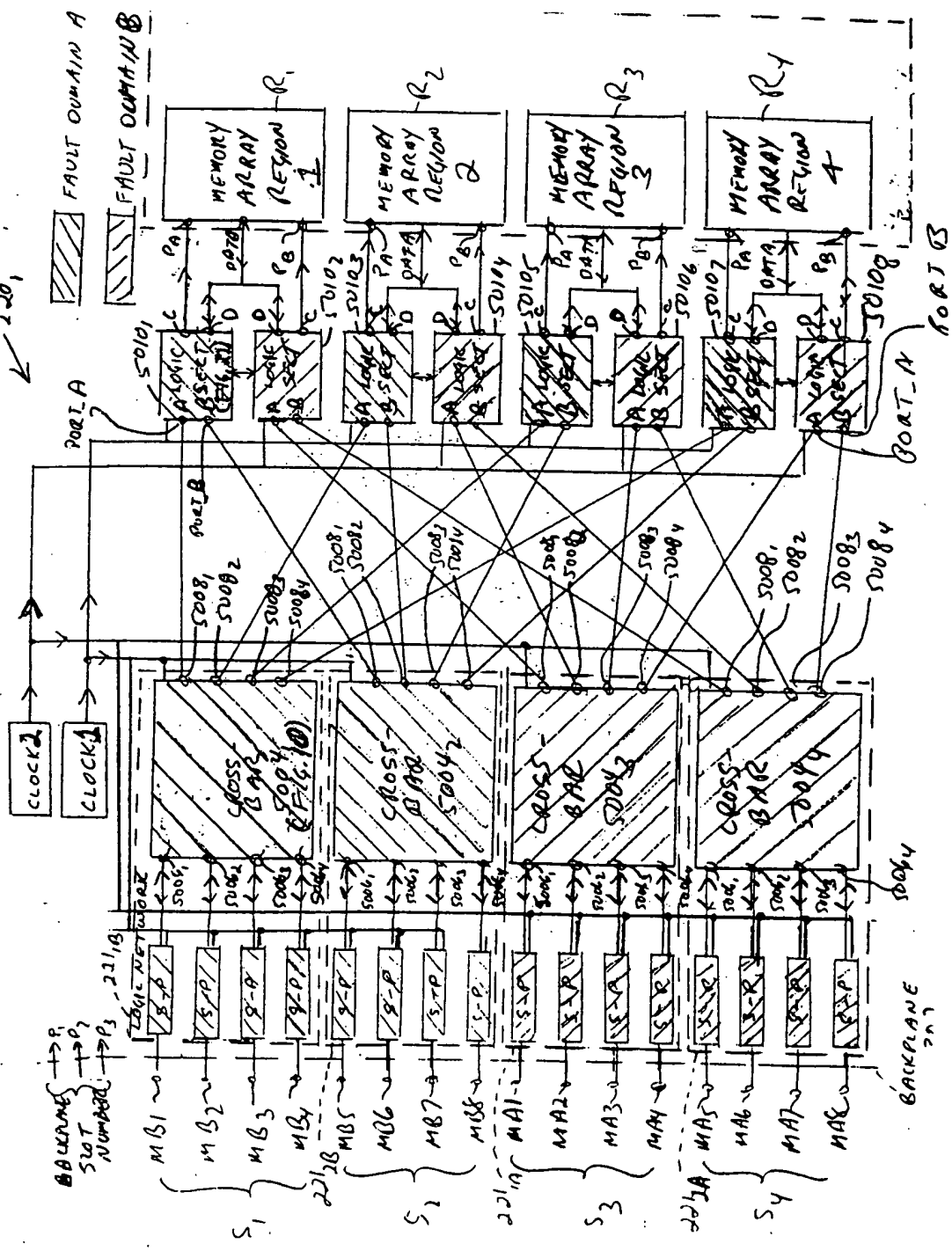

FAULT DOMAIN A
FAULT DOMAIN B
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
PORT_A
PORT_B
CLOCK2
CLOCK1
CROSS BAR SD04
CROSS BAR SD02
CROSS BAR SD03
CROSS BAR SD04
BACKPLANE

FIG. 9

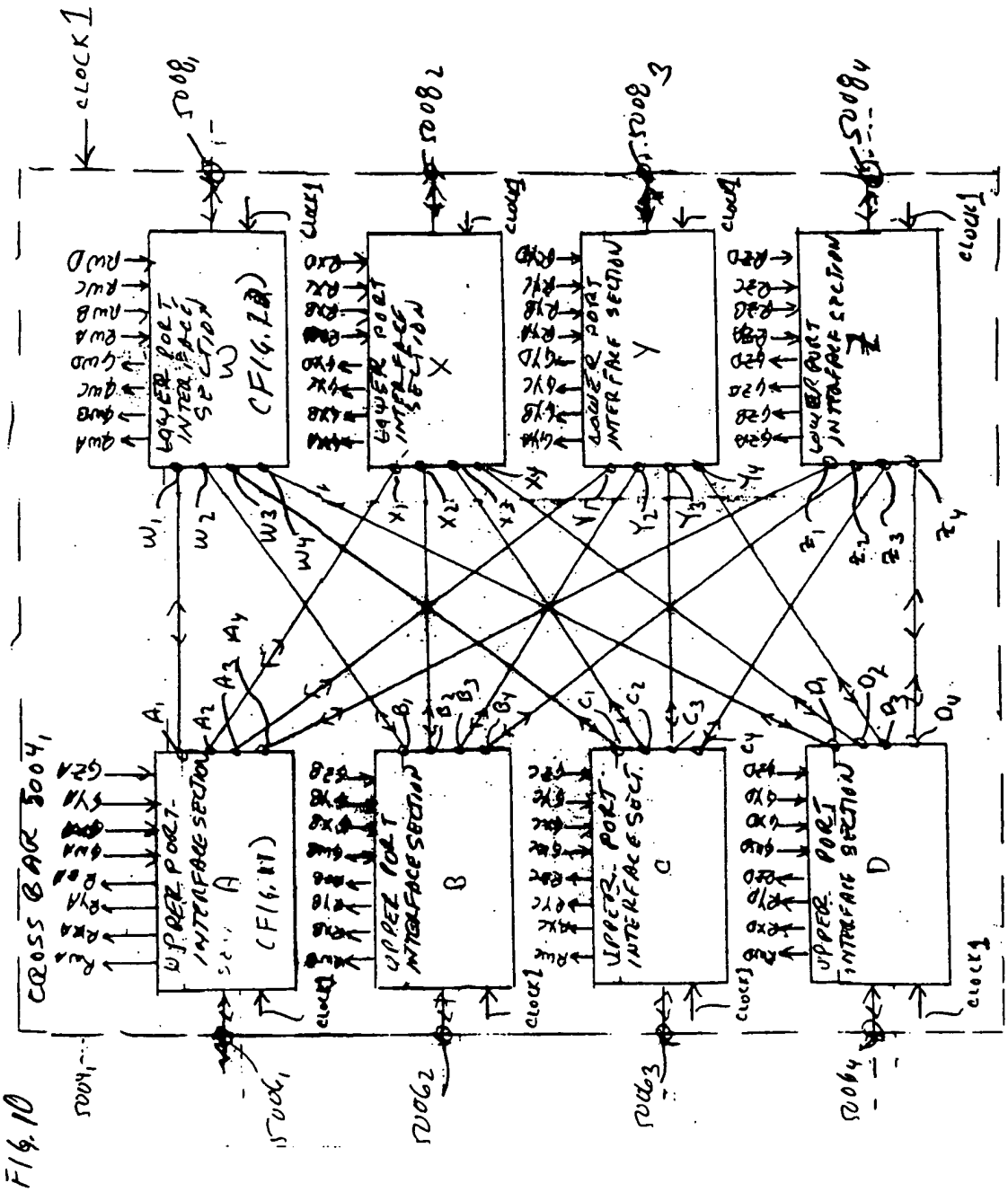

CLOCK 1
CROSS BAR SWITCH
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECT. C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
SDOB1
SDOB2
SDOB3
SDOB4
SDOA1
SDOA2
SDOA3
SDOA4
CLOCK1

FIG. 10

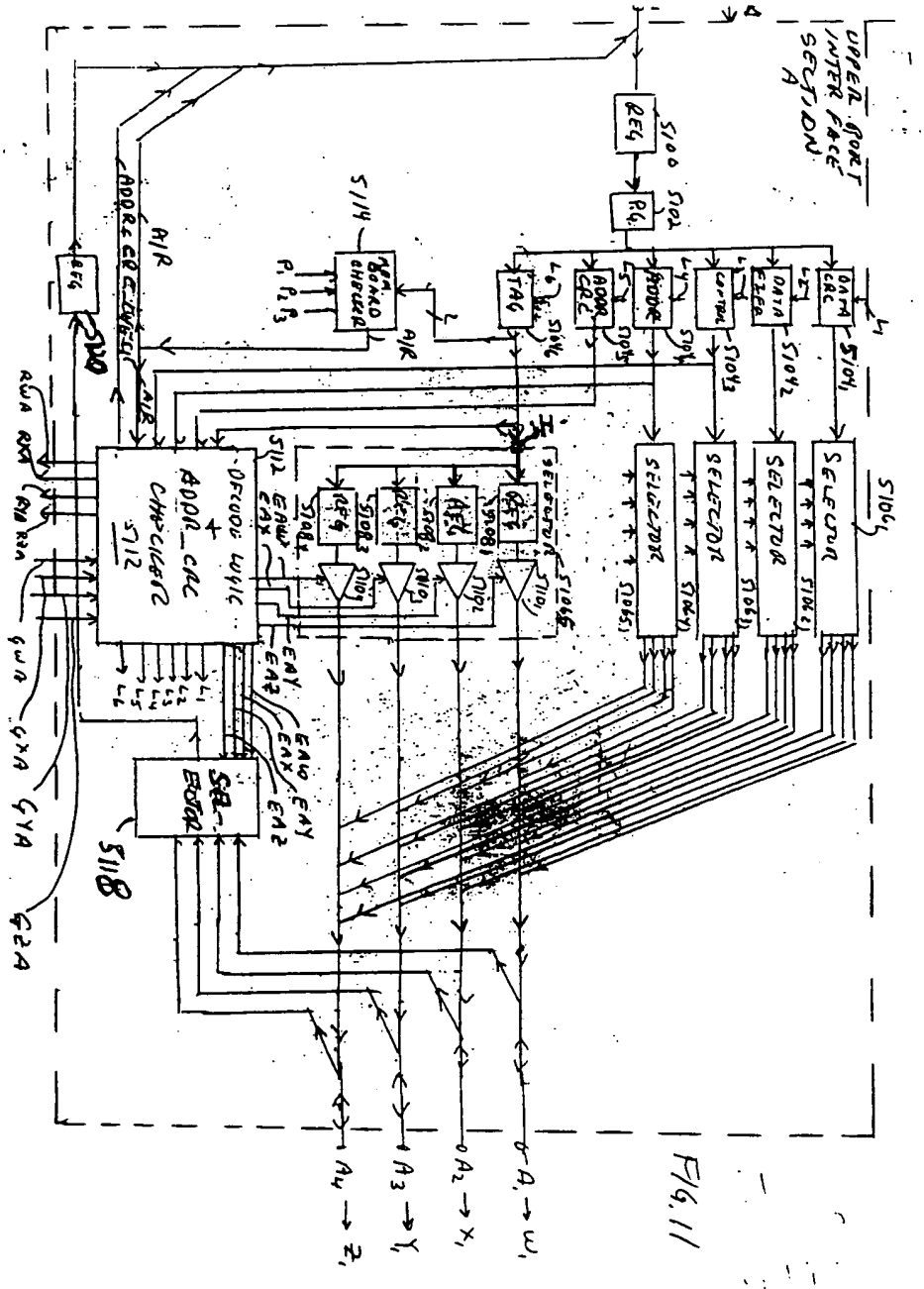

UPPER PORT INTER FACE SECTION
A
REG
5100
5102
R4
5114
BANKED ENERGY
P1 P2 P3
A/R
ADDRESS REGISTER
REG
TAG
ADDR CRC
ADDR
CONTROL
DATA REG
DATA CRC
5104
5103
5102
5101
SELECTOR
SELECTOR
SELECTOR
SELECTOR
5106
5112
DECODE WRITE ADDR_CRC CHECKER
5112
EAW
EAX
EAY
EAZ
EAW_EAY
EAX_EAZ
SEL
EQUAL
5118
G1A
G2A
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

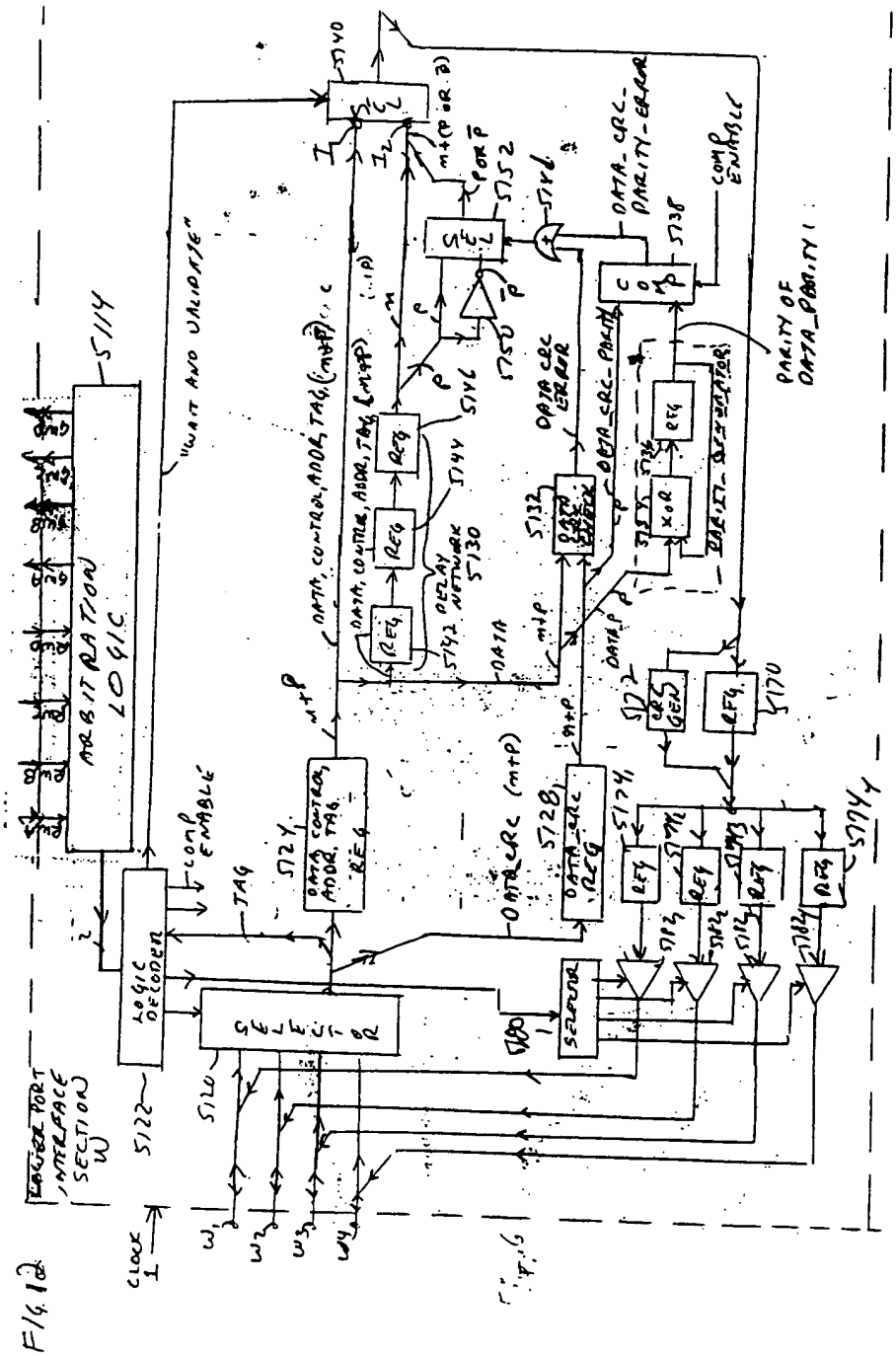

ARBITRATION LOGIC
"WAIT AND UNLOAD"
LOGIC DECODER
SELECTOR
DATA, CONTROL, ADDR, TAG, (m+P)
DELAY NETWORK
DATA CRC ERROR
DATA_CRC_PARITY
DATA_CRC_ERROR
PARITY OF DATA_PORT
COMP ENABLE
TAG
DATA
m+P
P
CLOCK
W1
W2
W3
W4

FIG. 1a

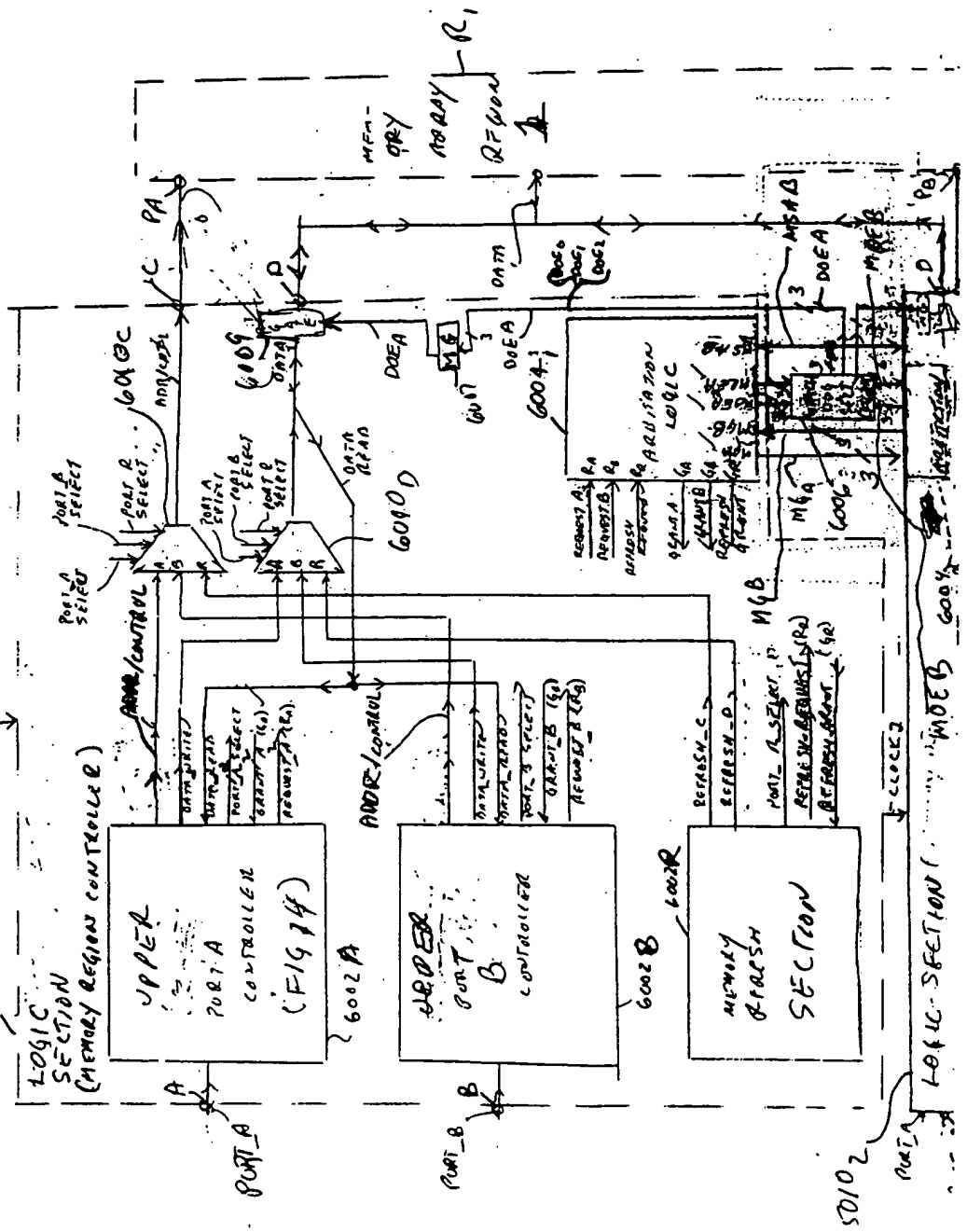
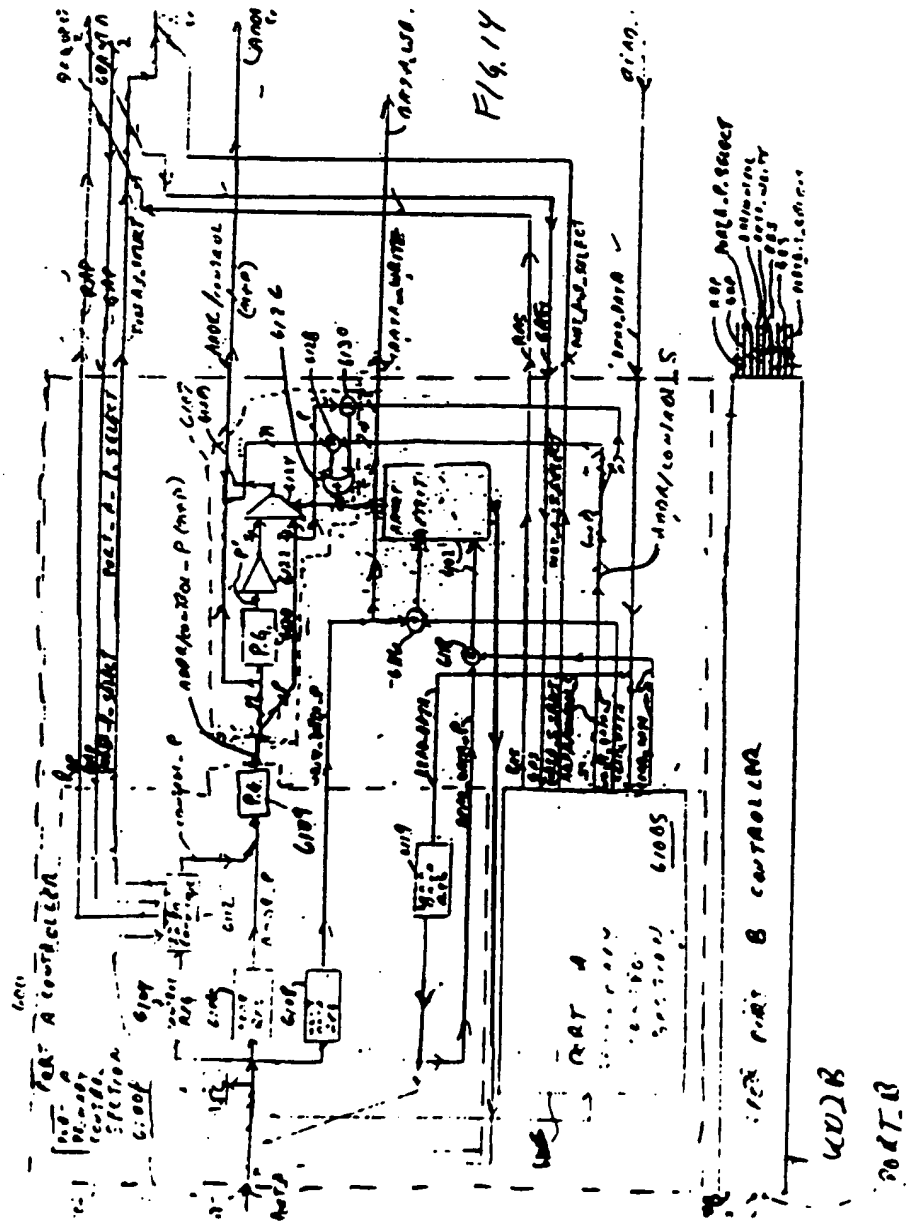
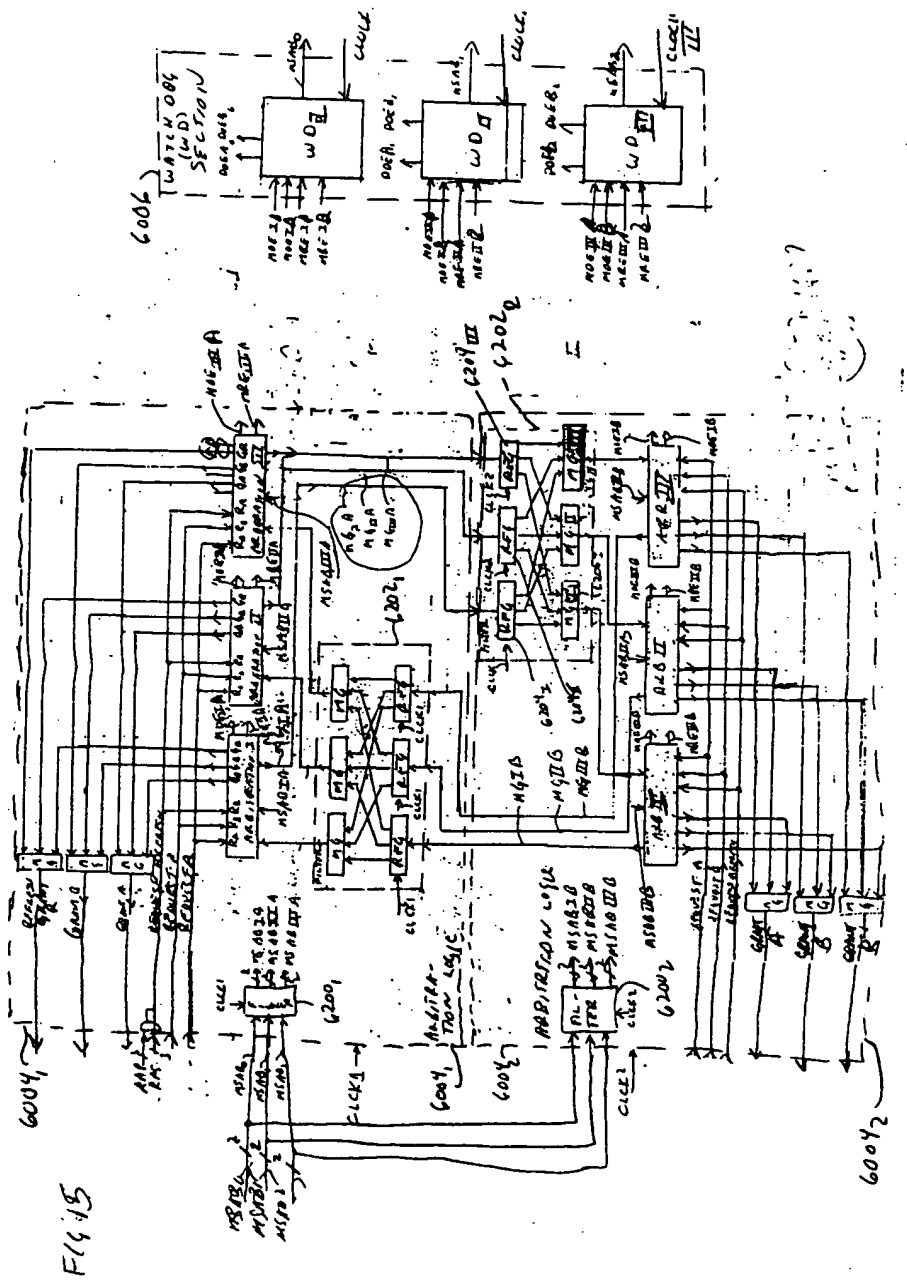

LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
CLOCK1
UPPER PORT A CONTROLLER (FIG 1F)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002C
PORT_A
PORT_B
5010
LOGIC SECTION
CLOCK2
MEMORY ARRAY
6004
6009
6010
ADDR/CONTROL
DATA READ
ARBITRATION LOGIC
REFRESH_C
PORT_A SELECT
PORT_B SELECT

FIG 1B





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METHOD FOR VALIDATING WRITE DA
TO A MEMORY
Application No. 09/746,496

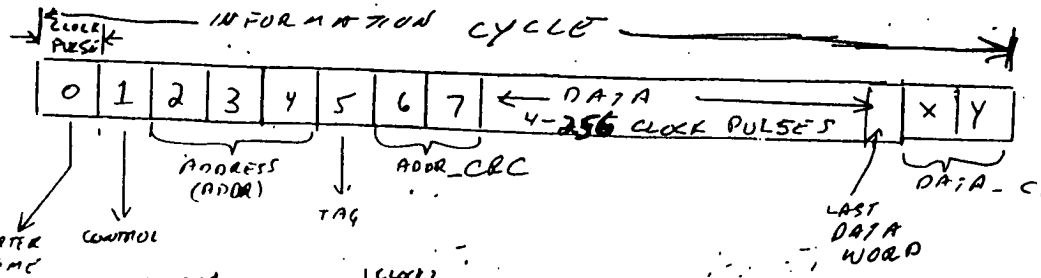

FIG. 16

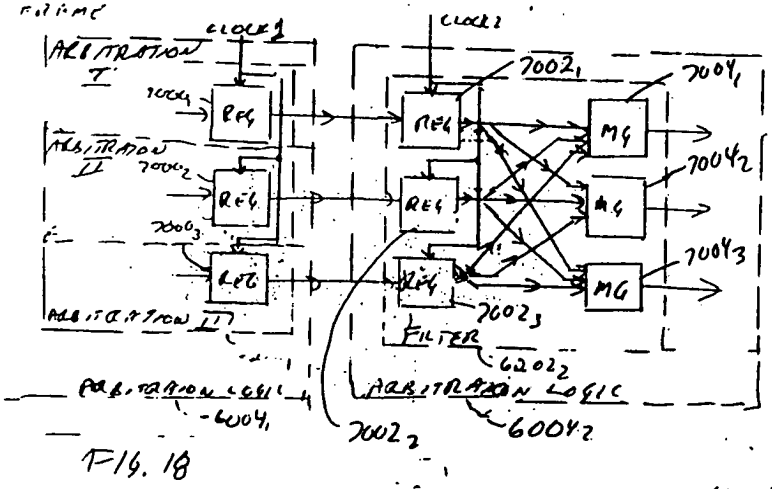

FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

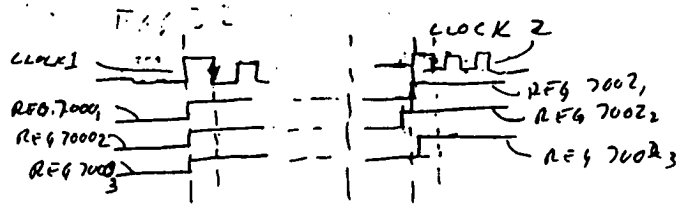
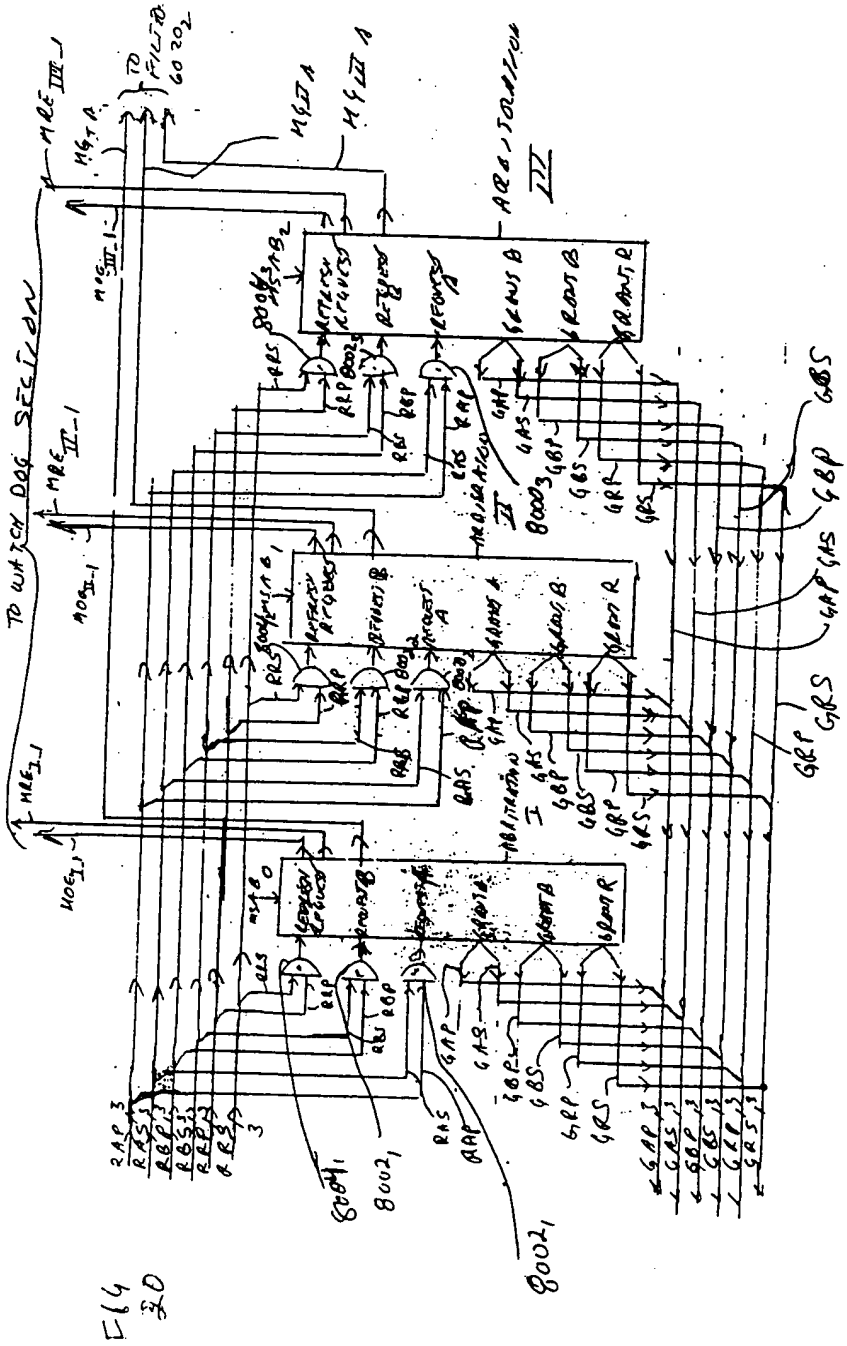
FIG. 19